A Bibliography of Publications about the RISC-V Open Source Computer Architecture

Nelson H. F. Beebe
University of Utah
Department of Mathematics, 110 LCB
155 S 1400 E RM 233
Salt Lake City, UT 84112-0090
USA

Tel: +1 801 581 5254
FAX: +1 801 581 4148

E-mail: beebe@math.utah.edu, beebe@acm.org,
beebe@computer.org (Internet)
WWW URL: https://www.math.utah.edu/~beebe/

27 September 2023
Version 1.15

Title word cross-reference

3 [ZBA+20].

000-core [DAKK19].

1 [DtEt22].

2-Petaflop [SB23]. **2017** [BBdD17]. **2019** [GD19, TBL19]. **2021** [IEE21]. **2022** [IEE22]. **24th** [BBdD17]. **26th** [TBL19]. **28th** [IEE21]. **29th** [IEE22].

30 [SB23]. **30-Teraflops** [SB23]. **30-Teraflops/W** [SB23]. **32-Bit** [MLPH23]. **32/64** [MG22]. **32/64-bit** [MG22].

4096-Core [ZSB21].

511-Core [DXT+18].

64-bit [MG22].

ABI [AVS+22]. **Abstraction** [HZS+19]. **Accelerated** [EAMK21]. **Accelerating** [DtEt22, DAKK19, ERGK21, KKC+16]. **Acceleration** [SB23]. **Accelerator** [BDdD19b, DXT+18, KBBA17, PGW+20, RSRT19]. **Achieving** [SZHB21]. **Agile** [LWC+16, PGW+20, XYT+23]. **ALU** [RTRM19]. **Android** [WWN23]. **application** [DL17]. **application-specific** [DL17]. **Applications** [CRRS22, MPU+23]. **Approach** [LWC+16]. **Architectural** [KKK+17a, KKK+17b, KKK+17c].

References

Amor:2022:RVI

[ABP22] Hela Belhadj Amor, Carolynn Bernier, and Zdeněk Přikryl. A RISC-V ISA extension for ultra-low power IoT wireless signal processing. *IEEE Transactions on Computers*, 71(4):766–778, April 2022. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Anonymous:2020:RVE

[Ano20] Anonymous. RISC-V embedded variant RV32E now fully supported by SEGGER's floating-point library. Web site, Septem-

ber 21, 2020. URL https://www.design-reuse.com/news/48672/segger-s-floating-point-library-risc-v-rv32e.html.

Adit:2022:PLT

[AS22] Neil Adit and Adrian Sampson. Performance left on the table: An evaluation of compiler autovectorization for RISC-V. *IEEE Micro*, 42(5):41–48, September/October 2022. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Alder:2022:FPU

[AVS+22] Fritz Alder, Jo Van Bulck, Jesse Spielman, David Oswald, and Frank Piessens. Faulty point unit: ABI poisoning attacks on trusted execution environments. *Digital Threats: Research and Practice (DTRAP)*, 3(2):13:1–13:26, June 2022. CODEN ???? ISSN 2692-1626 (print), 2576-5337 (electronic). URL https://dl.acm.org/doi/10.1145/3491264.

Burgess:2017:ISC

[BBdD17] Neil Burgess, Javier Bruguera, and Florent de Dinechin, editors. *2017 IEEE 24th Symposium on Computer Arithmetic (ARITH 24), London, UK, 24–26 July 2017*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017. ISBN 1-5386-1966-0 (print), 1-5386-1965-2, 1-5386-1964-4. ISSN 1063-6889. LCCN QA76.9.C62 S95 2017. URL http://ieeexplore.ieee.org/servlet/opac?punumber=8019911.

Bocco:2019:DPN

[BDdD19a] Andrea Bocco, Yves Durand, and Florent de Dinechin. Dynamic precision numerics using a variable-precision UNUM Type I HW coprocessor. In Takagi et al. [TBL19], pages 104–107. ISBN 1-72813-366-1. ISSN 1063-6889.

Bocco:2019:SSM

[BDdD19b] Andrea Bocco, Yves Durand, and Florent de Dinechin. SMURF: Scalar Multiple-precision Unum Risc-V Floating-point accelerator for scientific computing,. In Gustafson and Dimitrov [GD19], pages 1:1–1:8. ISBN 1-4503-7139-6. LCCN ???? URL https://hal.inria.fr/hal-02087098.

Bove:2023:BSS

[BF23] Davide Bove and Julian Funk. Basic secure services for standard RISC-V architectures. *Computers & Security*, 133 (??):??, October 2023. CODEN CPSEDU. ISSN 0167-4048 (print), 1872-6208 (electronic). URL http://www.sciencedirect.com/science/article/pii/S0167404823003255.

Biswas:2021:CSI

[Bis21] Arnab Kumar Biswas. Cryptographic software IP protection without compromising performance or timing side-

channel leakage. *ACM Transactions on Architecture and Code Optimization*, 18(2):20:1–20:20, March 2021. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://dl.acm.org/doi/10.1145/3443707`.

Bertaccini:2022:MNE

[BPF+22] Luca Bertaccini, Gianna Paulin, Tim Fischer, Stefan Mach, and Luca Benini. MiniFloat-NN and ExSdotp: an ISA extension and a modular open hardware unit for low-precision training on RISC-V cores. In IEEE [IEE22], pages 1–8. ISBN 1-66547-827-6, 1-66547-828-4. LCCN ????

Cococcioni:2022:LPP

[CRRS22] Marco Cococcioni, Federico Rossi, Emanuele Ruffaldi, and Sergio Saponara. A lightweight posit processing unit for RISC-V processors in deep neural network applications. *IEEE Transactions on Emerging Topics in Computing*, 10(4):1898–1908, October/December 2022. ISSN 2168-6750 (print), 2376-4562 (electronic).

Dogan:2019:ASU

[DAKK19] Halit Dogan, Masab Ahmad, Brian Kahne, and Omer Khan. Accelerating synchronization using moving compute to data model at 1,000-core multicore scale. *ACM Transactions on Architecture and Code Optimization*, 16(1):4:1–4:??, March 2019. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic).

Delshadtehrani:2018:NPM

[DEC+18] Leila Delshadtehrani, Schuyler Eldridge, Sadullah Canakci, Manuel Egele, and Ajay Joshi. Nile: a programmable monitoring coprocessor. *IEEE Computer Architecture Letters*, 17 (1):92–95, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Dietrich:2017:OVA

[DL17] Christian Dietrich and Daniel Lohmann. OSEK-V: application-specific RTOS instantiation in hardware. *ACM SIGPLAN Notices*, 52(4):111–120, May 2017. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Ditzel:2022:AMR

[DtEt22] David R. Ditzel and the Esperanto team. Accelerating ML recommendation with over 1,000 RISC-V/Tensor processors on Esperanto's ET-SoC-1 chip. *IEEE Micro*, 42(3): 31–38, May/June 2022. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Davidson:2018:COS

[DXT+18] Scott Davidson, Shaolin Xie, Christopher Torng, Khalid Al-Hawai, Austin Rovinski, Tutu Ajayi, Luis Vega, Chun Zhao, Ritchie Zhao, Steve Dai, Aporva Amarnath, Bandhav Veluri, Paul Gao, Anuj Rao, Gai Liu,

Rajesh K. Gupta, Zhiru Zhang, Ronald Dreslinski, Christopher Batten, and Michael Bedford Taylor. The Celerity open-source 511-core RISC-V tiered accelerator fabric: Fast architectures and design methodologies for fast chips. *IEEE Micro*, 38(2):30–41, March/April 2018. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `https://www.computer.org/csdl/mags/mi/2018/02/mmi2018020030-abs.html`.

Elkhatib:2021:ARV

[EAMK21] Rami Elkhatib, Reza Azarderakhsh, and Mehran Mozaffari-Kermani. Accelerated RISC-V for SIKE. In IEEE [IEE21], pages 131–138. ISBN 1-66542-293-9 (print), 1-66544-648-X (e-book). LCCN ????

Emil:2023:DEA

[EHN23] Demyana Emil, Mohammed Hamdy, and Gihan Nagib. Development an efficient AXI-interconnect unit between set of customized peripheral devices and an implemented dual-core RISC-V processor. *The Journal of Supercomputing*, 79(15): 17000–17019, October 2023. CODEN JOSUED. ISSN 0920-8542 (print), 1573-0484 (electronic). URL `https://link.springer.com/article/10.1007/s11227-023-05304-1`.

Eliahu:2021:MME

[ERGK21] Adi Eliahu, Ronny Ronen, Pierre-Emmanuel Gaillardon, and Shahar Kvatinsky. multiPULPly: a multiplication engine for accelerating neural networks on ultra-low-power architectures. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 17(2): 24:1–24:27, April 2021. CODEN ???? ISSN 1550-4832. URL `https://dl.acm.org/doi/10.1145/3432815`.

Feng:2022:RRV

[FHL+22] Lang Feng, Jiayi Huang, Luyi Li, Haochen Zhang, and Zhongfeng Wang. RvDfi: a RISC-V architecture with security enforcement by high performance complete data-flow integrity. *IEEE Transactions on Computers*, 71(10):2499–2512, October 2022. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Gruin:2023:MTP

[GCR+23] Alban Gruin, Thomas Carle, Christine Rochange, Hugues Cassé, and Pascal Sainrat. MINOTAuR: A timing predictable RISC-V core featuring speculative execution. *IEEE Transactions on Computers*, 72 (1):183–195, January 2023. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Gustafson:2019:PCN

[GD19] John Gustafson and Vassil Dimitrov, editors. *Proceedings of the Conference for Next Generation Arithmetic 2019, Singapore, March 2019*, ICPS. ACM

Press, New York, NY 10036, USA, 2019. ISBN 1-4503-7139-6. LCCN ????

Gomez:2023:HLV

[GMFC23] Constantino Gómez, Filippo Mantovani, Erich Focht, and Marc Casas. HPCG on long-vector architectures: Evaluation and optimization on NEC SX-Aurora and RISC-V. *Future Generation Computer Systems*, 143(??):152–162, June 2023. CODEN FGSEVI. ISSN 0167-739X (print), 1872-7115 (electronic). URL `http://www.sciencedirect.com/science/article/pii/S0167739X23000225`.

Greengard:2020:NWR

[Gre20] Samuel Greengard. News: Will RISC-V revolutionize computing? *Communications of the Association for Computing Machinery*, 63(5):30–32, May 2020. CODEN CACMA2. ISSN 0001-0782 (print), 1557-7317 (electronic). URL `https://dl.acm.org/doi/abs/10.1145/3386377`.

Garofalo:2021:XEEa

[GTC+21a] Angelo Garofalo, Giuseppe Tagliavini, Francesco Conti, Luca Benini, and Davide Rossi. XpulpNN: Enabling energy efficient and flexible inference of quantized neural networks on RISC-V based IoT end nodes. *IEEE Transactions on Emerging Topics in Computing*, 9 (3):1489–1505, July/September 2021. ISSN 2168-6750 (print), 2376-4562 (electronic). See [GTC+21b].

Garofalo:2021:XEEb

[GTC+21b] Angelo Garofalo, Giuseppe Tagliavini, Francesco Conti, Luca Benini, and Davide Rossi. XpulpNN: Enabling energy efficient and flexible inference of quantized neural networks on RISC-V based IoT end nodes. In IEEE [IEE21], page 53. ISBN 1-66542-293-9 (print), 1-66544-648-X (e-book). LCCN ???? See [GTC+21a].

Horne:2020:GSF

[Hor20] Mitchell Horne. Getting started with FreeBSD/RISC-V. *FreeBSD Journal*, ??(??):12–17, January/February 2020. URL `https://freebsdfoundation.org/wp-content/uploads/2020/03/Getting-Started-With-FreeBSD-RISC-V.pdf`.

Horne:2021:RQ

[Hor21a] Mitchell Horne. riscv/QEMU. Web site, June 8, 2021. URL `https://wiki.freebsd.org/riscv/QEMU`. See also [Hor20].

Horne:2021:S

[Hor21b] Mitchell Horne. Spike. Web site, June 8, 2021. URL `https://wiki.freebsd.org/riscv/Spike`.

Huang:2019:ILA

[HZS+19] Bo-Yuan Huang, Hongce Zhang, Pramod Subramanyan, Yakir Vizel, Aarti Gupta, and Sharad

Malik. Instruction-level abstraction (ILA): a uniform specification for system-on-chip (SoC) verification. *ACM Transactions on Design Automation of Electronic Systems*, 24(1):10:1–10:??, January 2019. CODEN ATASFO. ISSN 1084-4309 (print), 1557-7309 (electronic).

IEEE:2021:ISC

[IEE21] IEEE, editor. *2021 IEEE 28th Symposium on Computer Arithmetic: ARITH 2021: virtual conference, 14–16 June 2021: proceedings*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021. ISBN 1-66542-293-9 (print), 1-66544-648-X (e-book). LCCN ????

IEEE:2022:ISC

[IEE22] IEEE, editor. *2022 IEEE 29th Symposium on Computer Arithmetic: ARITH 2022: virtual conference, 12–14 September 2022: proceedings*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022. ISBN 1-66547-827-6, 1-66547-828-4. LCCN ????

Jin:2023:SBS

[JHQ23] Hai Jin, Zhuo He, and Weizhong Qiang. SpecTerminator: Blocking speculative side channels based on instruction classes on RISC-V. *ACM Transactions on Architecture and Code Optimization*, 20(1):15:1–15:??, March 2023. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://dl.acm.org/doi/10.1145/3566053`.

Koenig:2017:HAC

[KBBA17] Jack Koenig, David Biancolin, Jonathan Bachrach, and Krste Asanovic. A hardware accelerator for computing an exact dot product. In Burgess et al. [BBdD17], pages 114–121. ISBN 1-5386-1966-0 (print), 1-5386-1965-2, 1-5386-1964-4. ISSN 1063-6889. LCCN QA76.9.C62 S95 2017. URL `http://ieeexplore.ieee.org/servlet/opac?punumber=8019911`.

Kapre:2017:HDR

[KG17] Nachiket Kapre and Jan Gray. Hoplite: a deflection-routed directional torus NoC for FPGAs. *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 10(2):14:1–14:??, April 2017. CODEN ???? ISSN 1936-7406 (print), 1936-7414 (electronic).

Kuo:2023:RVG

[KGHRM23] Yao-Ming Kuo, Francisco García-Herrero, Oscar Ruano, and Juan Antonio Maestro. RISC-V Galois Field ISA extension for non-binary error-correction codes and classical and post-quantum cryptography. *IEEE Transactions on Computers*, 72 (3):682–692, March 2023. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Kim:2016:SCD

[KKC+16] Channoh Kim, Sungmin Kim, Hyeon Gyu Cho, Dooyoung Kim, Jaehyeok Kim, Young H. Oh, Hakbeom Jang, and Jae W. Lee. Short-circuit dispatch: accelerating virtual machine interpreters on embedded processors. *ACM SIGARCH Computer Architecture News*, 44(3):291–303, June 2016. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

Kim:2017:TAAa

[KKK+17a] Channoh Kim, Jaehyeok Kim, Sungmin Kim, Dooyoung Kim, Namho Kim, Gitae Na, Young H. Oh, Hyeon Gyu Cho, and Jae W. Lee. Typed architectures: Architectural support for lightweight scripting. *ACM SIGARCH Computer Architecture News*, 45(1):77–90, March 2017. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

Kim:2017:TAAb

[KKK+17b] Channoh Kim, Jaehyeok Kim, Sungmin Kim, Dooyoung Kim, Namho Kim, Gitae Na, Young H. Oh, Hyeon Gyu Cho, and Jae W. Lee. Typed architectures: Architectural support for lightweight scripting. *Operating Systems Review*, 51(2):77–90, June 2017. CODEN OSRED8. ISSN 0163-5980 (print), 1943-586X (electronic).

Kim:2017:TAAc

[KKK+17c] Channoh Kim, Jaehyeok Kim, Sungmin Kim, Dooyoung Kim, Namho Kim, Gitae Na, Young H. Oh, Hyeon Gyu Cho, and Jae W. Lee. Typed architectures: Architectural support for lightweight scripting. *ACM SIGPLAN Notices*, 52(4):77–90, April 2017. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Lee:2016:AAB

[LWC+16] Yunsup Lee, Andrew Waterman, Henry Cook, Brian Zimmer, Ben Keller, Alberto Puggelli, Jaehwa Kwak, Ruzica Jevtic, Stevo Bailey, Milovan Blagojevic, Pi-Feng Chiu, Rimas Avizienis, Brian Richards, Jonathan Bachrach, David Patterson, Elad Alon, Bora Nikolic, and Krste Asanovic. An agile approach to building RISC-V microprocessors. *IEEE Micro*, 36(2):8–20, March/April 2016. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://www.computer.org/csdl/mags/mi/2016/02/mmi2016020008-abs.html`.

Mariotti:2022:WVB

[MG22] Gianfranco Mariotti and Roberto Giorgi. `WebRISC-V`: a 32/64-bit RISC-V pipeline simulation tool. *SoftwareX*, 18(??):??, June 2022. CODEN ???? ISSN 2352-7110. URL `http://www.`

sciencedirect.com/science/article/pii/S235271102200070X.

Ma:2023:DSB

[MLPH23] Khai-Minh Ma, Duc-Hung Le, Cong-Kha Pham, and Trong-Thuc Hoang. Design of an SoC based on 32-bit RISC-V processor with low-latency lightweight cryptographic cores in FPGA. *Future Internet*, 15 (5):186, May 19, 2023. CODEN ???? ISSN 1999-5903. URL https://www.mdpi.com/1999-5903/15/5/186.

Mallasen:2022:POSa

[MMD+22a] David Mallasén, Raul Murillo, Alberto A. Del Barrio, Guillermo Botella, Luis Piñuel, and Manuel Prieto-Matias. PERCIVAL: Open-source posit RISC-V core with quire capability. *IEEE Transactions on Emerging Topics in Computing*, 10 (3):1241–1252, July/September 2022. ISSN 2168-6750 (print), 2376-4562 (electronic).

Mallasen:2022:POSb

[MMD+22b] David Mallasén, Raul Murillo, Alberto A. Del Barrio, Guillermo Botella, Luis Piñuel, and Manuel Prieto-Matias. PERCIVAL: Open-source posit RISC-V core with quire capability. In IEEE [IEE22], page 66. ISBN 1-66547-827-6, 1-66547-828-4. LCCN ???? Authors and title only. See [MMD+22a].

Minervini:2023:VAE

[MPU+23] Francesco Minervini, Oscar Palomar, Osman Unsal, Enrico Reggiani, Josue Quiroga, Joan Marimon, Carlos Rojas, Roger Figueras, Abraham Ruiz, Alberto Gonzalez, Jonnatan Mendoza, Ivan Vargas, César Hernandez, Joan Cabre, Lina Khoirunisya, Mustapha Bouhali, Julian Pavon, Francesc Moll, Mauro Olivieri, Mario Kovac, Mate Kovac, Leon Dragic, Mateo Valero, and Adrian Cristal. Vitruvius+: an area-efficient RISC-V decoupled vector coprocessor for high performance computing applications. *ACM Transactions on Architecture and Code Optimization*, 20(2):28:1–28:??, June 2023. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL https://dl.acm.org/doi/10.1145/3575861.

Petrisko:2020:BAO

[PGW+20] D. Petrisko, F. Gilani, M. Wyse, D. C. Jung, S. Davidson, P. Gao, C. Zhao, Z. Azad, S. Canakci, B. Veluri, T. Guarino, A. Joshi, M. Oskin, and M. B. Taylor. BlackParrot: An agile open-source RISC-V multicore for accelerator SoCs. *IEEE Micro*, 40 (4):93–102, July/August 2020. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Patterson:2017:RVR

[PW17] David Patterson and Andrew Waterman. *The RISC-V*

Reader: An Open Architecture Atlas. Strawberry Canyon, San Francisco, CA, USA, 2017. ISBN 0-9992491-1-8. xiv + 180 pp. LCCN QA76.9.A73 P388 2017.

Rogers:2019:SLB

[RSRT19] Samuel Rogers, Joshua Slycord, Ronak Raheja, and Hamed Tabkhi. Scalable LLVM-based accelerator modeling in gem5. *IEEE Computer Architecture Letters*, 18(1):18–21, January/ June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Ramos:2019:APM

[RTRM19] A. Ramos, R. G. Toral, P. Reviriego, and J. A. Maestro. An ALU protection methodology for soft processors on SRAM-based FPGAs. *IEEE Transactions on Computers*, 68(9):1404–1410, September 2019. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Snelgrove:2023:SPT

[SB23] Martin Snelgrove and Robert Beachler. speedAI240: a 2-petaflop, 30-Teraflops/W at-memory inference acceleration device with 1456 RISC-V cores. *IEEE Micro*, 43(3):58–63, May/ June 2023. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

SEGGER:2020:SFP

[SEG20] SEGGER Microcontroller. SEGGER floating-point library. Web site., January 2020. URL `https://www.segger.com/products/development-tools/runtime-library/technology/floating-point-library/`.

Sa:2022:FLR

[SMP22] Bruno Sá, José Martins, and Sandro Pinto. A first look at RISC-V virtualization from an embedded systems perspective. *IEEE Transactions on Computers*, 71(9):2177–2190, September 2022. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Saarinen:2022:DRV

[SNM22] Markku-Juhani O. Saarinen, G. Richard Newell, and Ben Marshall. Development of the RISC-V entropy source interface. *Journal of Cryptographic Engineering*, 12(4):371–386, November 2022. CODEN ???? ISSN 2190-8508 (print), 2190-8516 (electronic). URL `https://link.springer.com/article/10.1007/s13389-021-00275-6`.

Schuiki:2021:SSR

[SZHB21] F. Schuiki, F. Zaruba, T. Hoefler, and L. Benini. Stream semantic registers: A lightweight RISC-V ISA extension achieving full compute utilization in single-issue cores. *IEEE Transactions on Computers*, 70(2): 212–227, February 2021. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Szkandera:2021:BYO

[Szk21] Filip Szkandera. Build your own RISC-V CPU: Even homebrew processors can use hot new tech. *IEEE Spectrum*, 58 (6):16–18, June 2021. CODEN IEESAM. ISSN 0018-9235 (print), 1939-9340 (electronic).

Takagi:2019:ISC

[TBL19] Naofumi Takagi, Sylvie Boldo, and Martin Langhammer, editors. *2019 IEEE 26th Symposium on Computer Arithmetic ARITH-26 (2019), Kyoto, Japan, 10–12 June 2019*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, June 2019. ISBN 1-72813-366-1. ISSN 1063-6889.

Tran:2023:TFP

[TDH+23] Thai-Ha Tran, Ba-Anh Dao, Trong-Thuc Hoang, Van-Phuc Hoang, and Cong-Kha Pham. Transition factors of power consumption models for CPA attacks on cryptographic RISC-V SoC. *IEEE Transactions on Computers*, 72(9):2689–2700, September 2023. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Tiwari:2019:PPE

[TGRK19] Sugandha Tiwari, Neel Gala, Chester Rebeiro, and V. Kamakoti. PERI: A posit enabled RISC-V core. *arXiv.org*, ??(??):1–14, November 2019. URL `https://arxiv.org/pdf/1908.01466.pdf`.

Tiwari:2021:PCP

[TGRK21] Sugandha Tiwari, Neel Gala, Chester Rebeiro, and V. Kamakoti. PERI: a configurable posit enabled RISC-V core. *ACM Transactions on Architecture and Code Optimization*, 18(3):25:1–25:26, June 2021. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://dl.acm.org/doi/10.1145/3446210`.

Tan:2016:NVC

[TMK+16] Yong Kiam Tan, Magnus O. Myreen, Ramana Kumar, Anthony Fox, Scott Owens, and Michael Norrish. A new verified compiler backend for CakeML. *ACM SIGPLAN Notices*, 51(9): 60–73, September 2016. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Trippel:2017:TMMa

[TML+17a] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. TriCheck: Memory model verification at the trisection of software, hardware, and ISA. *ACM SIGARCH Computer Architecture News*, 45(1):119–133, March 2017. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

Trippel:2017:TMMb

[TML+17b] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi.

TriCheck: Memory model verification at the trisection of software, hardware, and ISA. *Operating Systems Review*, 51 (2):119–133, June 2017. CODEN OSRED8. ISSN 0163-5980 (print), 1943-586X (electronic).

Trippel:2017:TMMc

[TML+17c] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. TriCheck: Memory model verification at the trisection of software, hardware, and ISA. *ACM SIGPLAN Notices*, 52(4):119–133, April 2017. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

Talpes:2023:MDT

[TSW+23] Emil Talpes, Debjit Das Sarma, Doug Williams, Sahil Arora, Thomas Kunjan, Benjamin Floering, Ankit Jalote, Christopher Hsiong, Chandrasekhar Poorna, Vaidehi Samant, John Sicilia, Anantha Kumar Nivarti, Raghuvir Ramachandran, Tim Fischer, Ben Herzberg, Bill McGee, Ganesh Venkataramanan, and Pete Banon. The microarchitecture of DOJO, Tesla's exa-scale computer. *IEEE Micro*, 43(3):31–39, May/June 2023. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Vijaykumar:2022:MPO

[VOK+22] Nandita Vijaykumar, Ataberk Olgun, Konstantinos Kanellopoulos, F. Nisa Bostanci, Hasan Hassan, Mehrshad Lotfi, Phillip B. Gibbons, and Onur Mutlu. `MetaSys`: a practical open-source metadata management system to implement and evaluate cross-layer optimizations. *ACM Transactions on Architecture and Code Optimization*, 19(2):26:1–26:29, June 2022. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://dl.acm.org/doi/10.1145/3505250`.

Wen:2023:WCP

[WWN23] Elliott Wen, Gerald Weber, and Suranga Nanayakkara. WasmAndroid: a cross-platform runtime for native programming languages on Android. *ACM Transactions on Embedded Computing Systems*, 22(1): 4:1–4:??, January 2023. CODEN ???? ISSN 1539-9087 (print), 1558-3465 (electronic). URL `https://dl.acm.org/doi/10.1145/3530286`.

Xu:2023:TDH

[XYT+23] Yinan Xu, Zihao Yu, Dan Tang, Ye Cai, Dandan Huan, Wei He, Ninghui Sun, and Yungang Bao. Toward developing high-performance RISC-V processors using agile methodology. *IEEE Micro*, 43(4):98–106, July/August 2023. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Yang:2023:ATF

[YCL+23] Chun-Chieh Yang, Yi-Ru Chen,

Hui-Hsin Liao, Yuan-Ming Chang, and Jenq-Kuen Lee. Auto-tuning fixed-point precision with TVM on RISC-V packed SIMD extension. *ACM Transactions on Design Automation of Electronic Systems*, 28(3):33:1–33:??, May 2023. CODEN ATASFO. ISSN 1084-4309 (print), 1557-7309 (electronic). URL `https://dl.acm.org/doi/10.1145/3569939`.

Zhu:2020:HIR

[ZBA+20] Lingjun Zhu, Lennart Bamberg, Anthony Agnesina, Francky Catthoor, Dragomir Milojevic, Manu Komalan, Julien Ryckaert, Alberto Garcia-Ortiz, and Sung Kyu Lim. Heterogeneous 3D integration for a RISC-V system with STT-MRAM. *IEEE Computer Architecture Letters*, 19(1):51–54, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).

Zeeb:2022:RV

[Zee22] Bjoern Zeeb. RISC-V. Web site, June 26, 2022. URL `https://wiki.freebsd.org/riscv`.

Zhang:2022:TMT

[ZHLR22] Jipeng Zhang, Junhao Huang, Zhe Liu, and Sujoy Sinha Roy. Time-memory trade-offs for Saber+ on memory-constrained RISC-V platform. *IEEE Transactions on Computers*, 71(11):2996–3007, November 2022. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

Zaruba:2021:MCR

[ZSB21] F. Zaruba, F. Schuiki, and L. Benini. Manticore: A 4096-core RISC-V chiplet architecture for ultraefficient floating-point computing. *IEEE Micro*, 41(2):36–42, March/April 2021. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Zhang:2019:CBB

[ZWB19] S. Zhang, A. Wright, and T. Bourgeat. Composable building blocks to open up processor design. *IEEE Micro*, 39(3):47–55, May/June 2019. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

Zhang:2020:MRB

[ZZB+20] Jialiang Zhang, Yue Zha, Nicholas Beckwith, Bangya Liu, and Jing Li. MEG: a RISCV-based system emulation infrastructure for near-data processing using FPGAs and high-bandwidth memory. *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 13(4):19:1–19:24, October 2020. CODEN ???? ISSN 1936-7406 (print), 1936-7414 (electronic). URL `https://dl.acm.org/doi/10.1145/3409114`.